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cont.

a gate electrode formed on the gate insulation film corresponding to the sidewall of the substrate;

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an insulation film formed on the gate insulation film between the gate electrode and the lower portion of the substrate; and

impurity regions in the active layer corresponding to the upper and lower portions of the substrate.

REMARKS

Claims 1-6 remain in this application.

Numerals 60a, 60b are now described on page 4 of the specification as impurity regions to correct the Examiner's objection.

Regarding the Section 112, first paragraph rejection of claim 3, the Examiner's attention is respectfully directed to insulation film 30 on the top surface of the stepped substrate. See Figs. 3B-3D. Therefore, claim 3 is supported by the specification.

Claims 1, 3, 4, and 6 stand rejected under 35 U.S.C. 102(e) as being anticipated by Kang; and claims 2 and 5 stand rejected under 35 U.S.C. 103 as being obvious in view of teachings of Kang. This rejection is respectfully traversed in light of the amendments to claim 1.

The Examiner relies on the illustration in Fig. 5 of Kang to anticipate claim 1. As now amended, claim 1 recites "a stepped substrate forming a

single Z-shaped cross section". This distinguishes over Kang in that it discloses a cavity in a substrate with two opposed Z-shaped configurations defining opposed vertical sidewalls.

In the present invention, an offset region is formed on the whole lower region of the sidewall and substrate corresponding to the insulating layer as a single region; and on the other hand, in the Kang patent, two offset regions are formed at the both side surfaces centering the insulating film. Relative to that of the Kang patent, the offset structure of the present invention can enhance the flow of the current through the channel.

Conclusion

In the event there are any matters remaining in this application, the Examiner is invited to contact Mr. Joseph A. Kolasch, Registration No. 22,463 at (703) 205-8000 in the Washington, D.C. area.

Pursuant to the provisions of 37 C.F.R. §§ 1.17 and 1.136(a), the Applicant hereby petitions for an extension of three (3) months to April 3, 2002 the period in which to file a response to the Office Action dated October 3, 2002. A check for the required extension fee of \$920.00 is enclosed herewith.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By James T. Eller #39,538
att Joseph A. Kolasch #22,463

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

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Attachment: Version with Markings to Show Changes Made

(Rev. 02/06/01)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning on page 4, line 10, has been amended as follows:

--FIG. 2 is a vertical cross-sectional view of a thin film transistor according to the present invention. As shown therein, a substrate 10 has a step formed on an upper surface thereof, and thus is provided with upper and lower portions 11, 12, and a sidewall 13 therebetween. An active layer 20 is formed on the upper and lower portions 11, 12, and on the sidewall 13. A gate insulation film 30 is formed on a part of the active layer 20 corresponding to the lower portion 12 and on a part of the active layer 20 corresponding to the sidewall 13. A gate electrode 42 is formed on the gate insulation film 30 corresponding to an upper part of the sidewall 13, and an insulation film 41 is formed on a part of the gate insulation film 30 corresponding to the lower portion 12 of the substrate 10 and on a part of the gate insulation film 30 corresponding to a lower part of the sidewall 13 of the substrate 10. Parts of the active layer 20, externally exposed on the upper and lower portions 11, 12 of the substrate 10, are respectively formed as impurity regions 60a and 60b. In addition, an additional insulation film (not shown) is formed on the upper and lower portions 11, 12, and on the sidewall 13.--

IN THE CLAIMS:

The claims have been amended as follows:

1. (amended) A thin film transistor, comprising:
 - a stepped substrate forming a single Z-shaped cross section provided with a sidewall between upper and lower portions thereof;
 - an active layer formed on the stepped substrate;
 - a gate insulation film formed on the active layer;
 - a gate electrode formed on the gate insulation film corresponding to the sidewall of the substrate;
 - an insulation film formed on the gate insulation film between the gate electrode and the lower portion of the substrate; and
 - impurity regions in the active layer corresponding to the upper and lower portions of the substrate.